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Question Paper Code : 40081

M.E./M.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018.

First Semester

Applied Electronics

AP 5151 – ADVANCED DIGITAL SYSTEM DESIGN

(Common to VLSI Design)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Write the differences between Moore and Mealy type of sequential circuits.

2. What is one-hot encoding?

3. When is the expected occurance of static and dynamic hazards take place?

4. Draw the state diagram for SR Latch.

5. Differentiate between truth table and D algorithm singular cover.

6. Specify the features of Boundary scan over other BISTs.

7. How does the field programmable address decoder differ from FPGA?

8. List the unique applications of sequential PAL devices.

9. Show the four kinds of tri state buffers.

10. How do the VHDL procedures differ from functions?

PART B — (5 × 13 = 65 marks)

11. (a) A general sequential circuit with input W, output Z with two state flip flops is shown below. Obtain the state assigned table and derive the logic expressions using K map reduction technique and implement the sequential circuit.

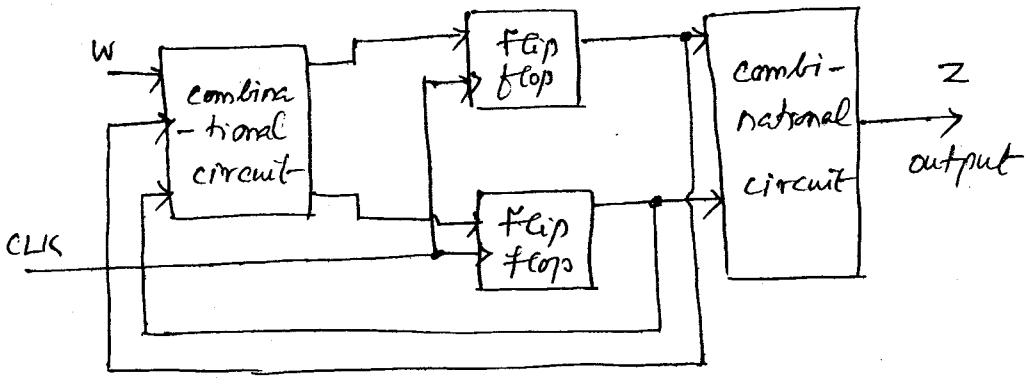

Figure 11 (a)

Or

(b) The sequence of input-output signals for a sequential circuit is given below. Assume W as the input and Z as the output. Draw the state diagram of an FSM that realizes the task and obtain the state table, state assigned table, the circuit and the timing diagram for the same.

Clock	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
W	0	1	0	1	1	0	1	1	1	0	1
Z	0	0	0	0	1	0	0	1	1	0	0

12. (a) Draw the basic circuit that is represented by the following expressions :

$$Y_1 = Y_1\overline{Y}_2 + W\overline{Y}_2 + \overline{W}_1\overline{W}_2Y_1$$

$$Y_2 = Y_1Y_2 + W_1Y_2 + W_2 + \overline{W}_1\overline{W}_2\,Y_1$$

$$Z = \overline{Y}_1\,Y_2$$

Obtain the excitation and flow tables. (13)

Or

(b) The initial flow table of a simple vending machine is given below. Analyze the merging procedures and arrive at the reduced flow table through primitive flow table. (13)

Present state	Next state DN				Output Z
	00	01	10	11	
A	Ⓐ	B	C	–	0
B	D	Ⓑ	–	–	0
C	A	–	Ⓒ	–	1
D	Ⓓ	E	F	–	0
E	A	Ⓔ	–	–	1
F	A	–	Ⓕ	–	1

13. (a) (i) For the logic circuit shown below, obtain the boolean difference with respect to x_2. (8)

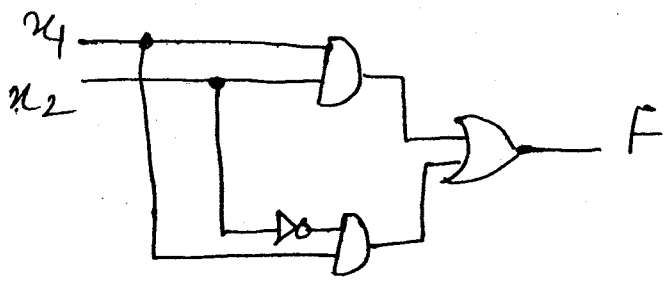

Figure 13 a (i)

(ii) Discuss the approaches that detect the multiple faults in combinational logic circuits. (5)

Or

(b) Draw the flow chart that depicts the operation of PODEM – test generation algorithm. Elaborate its back trace procedure. (13)

14. (a) Design a 4 bit binary counter using PAL. In the design process draw the state table, derive the logical equations, show the K map reduction and implement using PAL. (13)

Or

(b) With the internal structure block diagram of CLB, explain the modes of operation in Xilinx 4000 FPGA. (13)

15. (a) Write a VHDL program for a full adder module and show how to use the module as a component in a system that consists of four full adders connected to form a 4 bit binary adder. Define the structural description of the same. (13)

Or

(b) The general model of mealy sequential machine is given with its state table (13)

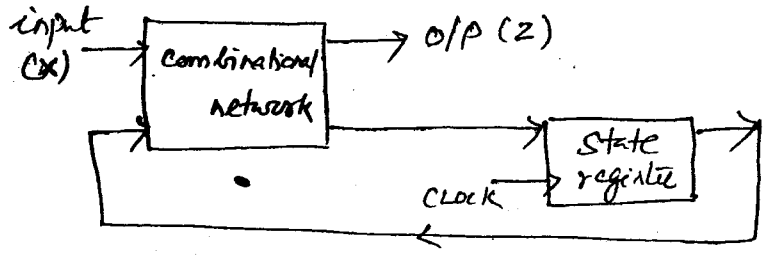

Figure 15 (b)

Present state	Next state		Output (z)	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
S_0	S_1	S_2	1	0
S_1	S_3	S_4	1	0
S_2	S_4	S_4	0	1
S_3	S_5	S_5	0	1
S_4	S_5	S_6	1	0
S_5	S_0	S_0	0	1
S_6	S_0	–	1	–

Write the behavioral model in VHDL for this mealy sequential network.

PART C — ($1 \times 15 = 15$ marks)

16. (a) Design a sequential traffic light controller for the intersection of "A" street and "B" street. Each street has traffic sensors, which detect the presence of vehicles approaching or stopped at the intersection. $S_a = 1$ indicates vehicle approaching on "A" and $S_b = 1$ for "B". "A" street is a main street and has a green light until a car approaches on "B". Then light changes and 'B' has green light. At the end of 50 seconds the light change back unless there is a car on B street and none on A. Then B gets extended time of 10S. Have three outputs of light $G_a Y_a R_a$ for A and $G_n Y_n R_n$ for B. Design the Moore graph and write the VHDL code. (15)

Or

(b) Devise a test to distinguish between two circuits that implement the following expressions

$f = x_1 x_2 x_3 + x_2 \bar{x}_3 x_4 + \bar{x}_1 \bar{x}_2 x_4 + \bar{x}_1 x_3 \bar{x}_4$

$g = (\bar{x}_1 + x_2)(x_3 + x_4)$