Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 47031

M.E./M.Tech. DEGREE EXAMINATION, JANUARY 2018
First Semester
Applied Electronics
AP5151 – ADVANCED DIGITAL SYSTEM DESIGN
(Common to M.E. VLSI Design)
(Regulations 2017)

Time : Three Hours Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Distinguish synchronous and asynchronous sequential logic circuits.
2. List out the elements present in the ASM chart.
3. Define : Hazards.
4. What do you mean by race around condition ?
5. What do you mean by fault simulation ? Also its types.
6. Draw the circuit diagram for 3-bit LFSR and its sequence.
7. Write down the features of FPGA.
8. List out the different types of Programming Logic Devices.
9. Write the Verilog code for half adder using gate level modelling.
10. Mention any four types of operators in Verilog HDL code.

PART – B **(5×13=65 Marks)**

11. a) Design a FSM for a single input and single output Mealy type FSM that produces an output of 1 if an input sequence it detects either 110 or 101 pattern. Overlapping sequences should be detected. **(13)**

(OR)

b) Design a serial adder Moore type FSM. **(13)**

12. a) Design a circuit that has an input w and output z, such that when the pulses are applied to w, the output z is equal to 0 if the numbers of previously applied pulses are even and z is equal to 1 if the numbers of pulses are odd. **(13)**

(OR)

b) Design a counter which counts the number of pulses on an input line w. **(13)**

13. a) Find out the test pattern generation for the function F = A + B' C using ATPG Algorithm. **(13)**

(OR)

b) Generate the test vector and signature analysis for the circuit under test using BIST algorithm. **(13)**

14. a) Explain about the structure of Xilinx 4000 CLB and I/O blocks with neat diagram. **(13)**

(OR)

b) Considering the following Boolean functions, design a combinational circuit using a PAL. **(13)**

$w(A, B, C, D) = \sum(2, 12, 13)$

$x(A, B, C, D) = \sum(7, 8, 9, 10, 11, 12, 13, 14, 15)$

$y(A, B, C, D) = \sum(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$

$z(A, B, C, D) = \sum(1, 2, 8, 12, 13)$.

15. a) Design and write the Verilog code for 4-bit Ripple carry adder using structural level modelling. **(13)**

(OR)

b) Design and write the Verilog code for 16 to 1 Multiplexer using 4 to 1 multiplexer circuit. **(13)**

PART – C **(15×1=15 Marks)**

16. a) Design a modulo-6 counter, which counts in the sequences 0, 1, 2, 3, 4, 5, 0, 1,.... The counter counts the clock pulse if its enable input w, is equal to 1. Use D flip-flops in your circuit. **(15)**

(OR)

b) Design and write the Verilog code for 8-bit ALU circuit which performs the basic arithmetic and logical operation. **(15)**

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