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Question Paper Code : 60056

M.E. DEGREE EXAMINATION, MAY/JUNE 2017.

Elective

Applied Electronics

AP 7001 — COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

(Common to M.E. VLSI Design)

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State the various performance metrices w.r.t computer design.
2. Define SIMD.
3. Define Orchestration.
4. State the significance of using dynamic scheduling.
5. Compare write-through and write-back caches.
6. List the commonly used memories with example.
7. List four categories of multiprocessors placed in all computers.
8. State the advantages of Different Communication Mechanisms.
9. Justify the need for multi core architecture with example.
10. Draw the IBM cell architecture.

PART B — (5 × 13 = 65 marks)

11. (a) Explain the parallel and scalable architecture with neat sketch.

Or

(b) Discuss the performance measuring and reporting of any two computers with case study.

12. (a) With neat flow diagram, explain the dynamic branch prediction with proper example and list the advantages and disadvantages over static branch prediction.

Or

(b) Discuss about Superscalar and very long instruction word processor with appropriate diagrams.

13. (a) Discuss about design of memory hierarchies and explain how the memory hierarchy will access during code refactoring with case study.

Or

(b) Explain about compiler optimisation and blocked algorithm optimisation to improve cache performance.

14. (a) Explain the two important cache coherency protocols by solving one coherence problem.

Or

(b) Draw and explain the multi processor and multi computer architecture.

15. (a) (i) Differentiate software and hardware multithreading approaches. (7)

(ii) Explain the models of memory consistency. (6)

Or

(b) Describe the architecture of the IBM cell processor in detail with appropriate diagrams.

PART C — (1 × 15 = 15 marks)

16. (a) Consider a simple example program with two phases. In the first phase, a single operation is performed independently on all points of a two-dimensional n-by-n grid, as in Ocean. In the second, the sum of the n^2 grid point values is computed. If we have p processors, we can assign n^2/p points to each processor and complete the first phase in parallel in time n^2/p. In the second phase, each processor can add each of its assigned n^2/p values into a global sum variable. What is the problem with this assignment, and how can we expose more concurrency?

Or

(b) In a uniprocessor with cache, the processor issues its memory access requests to cache controller (CC). In case of miss or write through, CC interacts with memory controller (MC). Draw the flow charts describing the operation of CC for a read and a write operation for:

(i) WBWA

(ii) WTWA

(iii) Write through without write allocation.